PATENT
Customer No. 22,852
Attorney Docket No. 04329.2343-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Atsushi YAGISHITA et al.	***Prior*** Group Art Unit: 2823
Div. of Application No.: 10/200,445, filed July 23, 2002	***Prior*** Examiner: Pham, Thanh V.
Filed: Herewith	
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	

Commissioner for Patents
Washington, DC 20231

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents listed on the attached PTO 1449. This Information Disclosure Statement is being filed concurrently with the above-referenced divisional application.

Copies of the listed documents were previously submitted in prior application Nos. 10/200,445, filing date July 23, 2002, and 09/609,713, filing date June 30, 2000 (now U.S. Patent No. 6,465,823), upon which Applicants rely for the benefits provided in 35 U.S.C. § 120. Applicants respectfully request that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim

in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the Office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: March 29, 2004

By: _____
Bryan S. Latham
Reg. No. 49,085

OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.2343-02	Div. of Appln. No.	10/200,445
Applicant	Atsushi YAGISHITA et al.		
Filing Date	Herewith	Prior Group:	2823

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		4,996,574	02/1991	Shirasaki			
		6,165,828	09/1998	Forbes et al.			
		6,177,299 B1	01/1998	Hsu et al.			

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		10-242477	09/1998	Japan			
		09162302 A	06/1997	Japan			
		03205869 A	09/1991	Japan			
		CN 1186346A	07/1998	People's Republic of China			
		05343687A	12/1993	Japan			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Assaderaghi, F., "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Trans. Electron Devices, Vol. 44, pp. 414-422, March 1997
	Wong et al., "A 1V CMOS Digital Circuits With Double-Gate-Driven MOSFET," IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE DIGEST OF TECHNICAL PAPERS, February 1997, pp. 292, 293, and 473

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce